XC95288XL High Performance CPLD

September 28, 1998 (Version 1.0)

Advance Product Specification

Features

- 6 ns pin-to-pin logic delays
- System frequency up to 151 MHz
- 288 macrocells with 6,400 usable gates
- Available in small footprint packages
  - 144-pin TQFP (117 user I/O pins)
  - 208-pin PQFP (168 user I/O pins)
  - 352-pin BGA (192 user I/O pins)
- Optimized for high-performance 3.3 V systems
  - Low power operation
  - 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
  - 3.3 V or 2.5 V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with 3 global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000 V
- Pin-compatible with 5 V-core XC95288 device in the 208-pin HQFP package

Description

The XC95288XL is a 3.3 V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of sixteen 54V18 Function Blocks, providing 6,400 usable gates with propagation delays of 6 ns. See Figure 2 for architecture overview.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

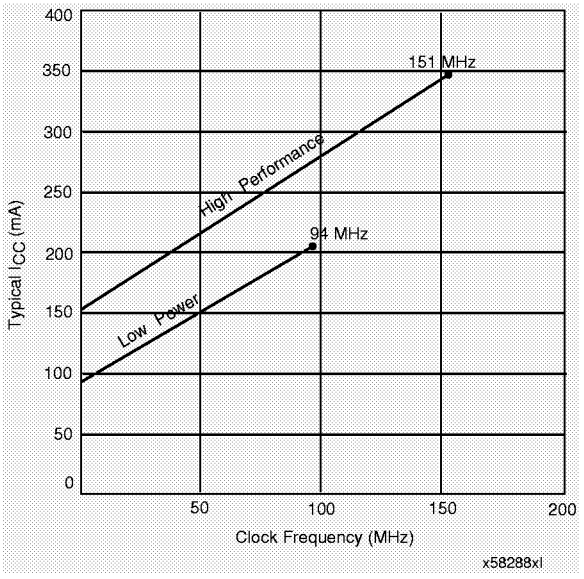


Figure 1: Typical I_{cc} vs. Frequency for XC95288XL

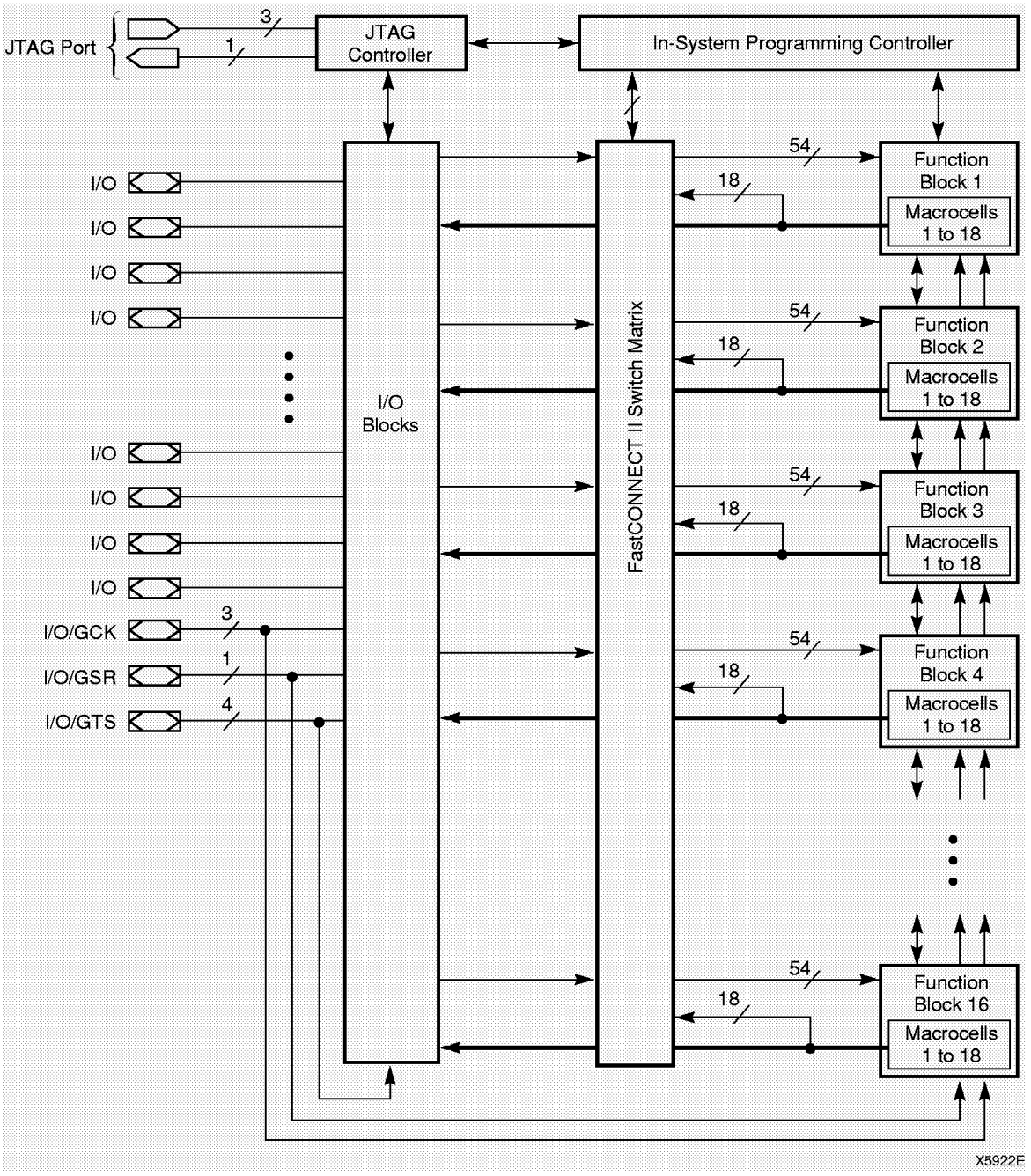


Figure 2: XC95288XL Architecture

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	+150	°C

Note 1: Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to +7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = -40°C to +85°C	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3 V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5 V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

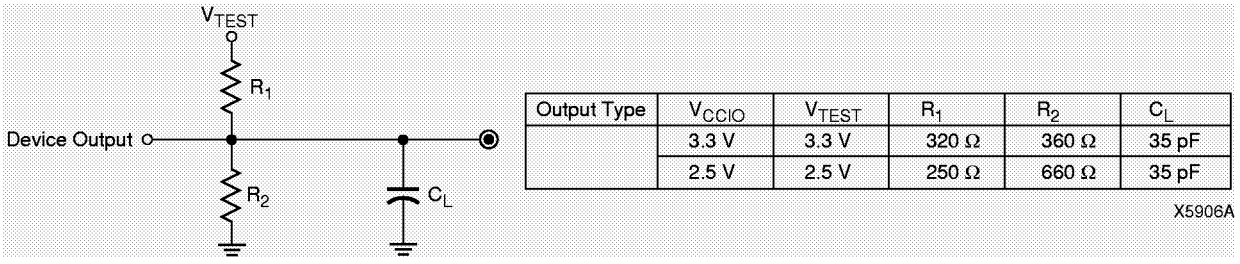
DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3 V outputs	I_{OH} = -4.0 mA	2.4		V
	Output high voltage for 2.5 V outputs	I_{OH} = -500 µA	90% V_{CCIO}		V
V_{OL}	Output low voltage for 3.3 V outputs	I_{OL} = 8.0 mA		0.4	V
	Output low voltage for 2.5 V outputs	I_{OL} = 500 µA		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		± 10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		± 10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	85(Typ)		mA

AC Characteristics

Symbol	Parameter	XC95288XL-6		XC95288XL-10		Units
		Min[1]	Max[1]	Min[1]	Max[1]	
t_{PD}	I/O to output valid		6.0		10.0	ns
t_{SU}	I/O setup time before GCK	4.1		6.5		ns
t_{H}	I/O hold time after GCK	0.0		0.0		ns
t_{CO}	GCK to output valid		4.3		5.8	ns
f_{SYSTEM}	Multiple FB internal operating frequency		151.5		100.0	MHz
t_{PSU}	I/O setup time before p-term clock input	2.1		2.1		ns
t_{PH}	I/O hold time after p-term clock input	2.0		4.4		ns
t_{PCO}	P-term clock output valid		6.3		10.2	ns
t_{OE}	GTS to output valid		4.5		7.0	ns
t_{OD}	GTS to output disable				7.0	ns
t_{POE}	Product term OE to output enabled		8.0		11.0	ns
t_{POD}	Product term OE to output disabled				11.0	ns
t_{AO}	GSR to output valid		10.8		14.5	ns
t_{PAO}	P-term S/R to output valid		11.6		15.3	ns
t_{WLH}	GCK pulse width (High or Low)	3.3		4.5		ns
t_{PLH}	P-term clock pulse width (High or Low)	6.0		7.0		ns
		Advance				

Note 1: Please contact Xilinx for up-to-date information on advance specifications.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3 V	3.3 V	320 Ω	360 Ω	35 pF
	2.5 V	2.5 V	250 Ω	660 Ω	35 pF

X5906A

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC95288XL-6		XC95288XL-10		Units
		Min[1]	Max[1]	Min[1]	Max[1]	
Buffer Delays						
t_{IN}	Input buffer delay		1.8		3.5	ns
t_{GCK}	GCK buffer delay		1.4		1.8	ns
t_{GSR}	GSR buffer delay		2.2		4.5	ns
t_{GTS}	GTS buffer delay		4.5		7.0	ns
t_{OUT}	Output buffer delay		2.4		3.0	ns
t_{EN}	Output buffer enable/disable delay		0.0		0.0	ns
Product Term Control Delays						
t_{PTCK}	Product term clock delay		1.6		2.7	ns
t_{PTSR}	Product term set/reset delay		1.2		1.8	ns
t_{PTTS}	Product term 3-state delay		6.2		7.5	ns
Internal Register and Combinatorial Delays						
t_{PDI}	Combinatorial logic propagation delay		0.6		1.7	ns
t_{SUI}	Register setup time	2.5		3.0		ns
t_{HI}	Register hold time	1.6		3.5		ns
t_{ECSU}	Register clock enable setup time	2.5		3.0		ns
t_{ECHO}	Register clock enable hold time	1.6		3.5		ns
t_{COI}	Register clock to output valid time		0.5		1.0	ns
t_{AOI}	Register async. S/R to output delay		6.2		7.0	ns
t_{RAI}	Register async. S/R recover before clock			10.0		ns
t_{LOGI}	Internal logic delay		1.2		1.8	ns
t_{LOGILP}	Internal low power logic delay		5.2		7.3	ns
Feedback Delays						
t_F	FastCONNECT II™ feedback delay		2.4		4.2	ns
Time Adders						
t_{PTA}	Incremental product term allocator delay		0.8		1.0	ns
t_{SLEW}	Slew-rate limited delay		3.5		4.5	ns
		Advance				

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

XC95288XL I/O Pins

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
1	1	–	–	–	861	
1	2	–	28	N26	858	
1	3	–	29	P25	855	
1	4	–	–	–	852	
1	5	20	30	P23	849	
1	6	21	31	P24	846	
1	7	–	–	–	843	
1	8	22	32	R26	840	
1	9	–	–	R25	837	
1	10	23	33	R24	834	
1	11	–	–	R23	831	
1	12	24	34	T26	828	
1	13	–	–	–	825	
1	14	25	35	T25	822	
1	15	26	36	T23	819	
1	16	–	–	–	816	
1	17	27	37	V26	813	
1	18	–	–	–	810	
2	1	–	–	–	807	
2	2	9	15	K23	804	
2	3	10	16	K24	801	
2	4	–	–	–	798	
2	5	11	17	J25	795	
2	6	12	18	L24	792	
2	7	–	–	–	789	
2	8	13	19	K25	786	
2	9	–	–	L25	783	
2	10	14	20	L26	780	
2	11	–	–	M23	777	
2	12	15	21	M24	774	
2	13	–	–	–	771	
2	14	16	22	M25	768	
2	15	17	23	M26	765	
2	16	–	–	–	762	
2	17	19	25	N25	759	
2	18	–	–	–	756	

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
3	1	–	–	–	753	
3	2	28	38	U24	750	
3	3	–	39	U23	747	
3	4	–	–	–	744	
3	5	–	40	Y26	741	
3	6	–	41	W25	738	
3	7	–	–	–	735	
3	8	–	43	AA26	732	
3	9	–	–	Y25	729	
3	10	30	44	Y24	726	[1]
3	11	–	–	AA25	723	
3	12	31	45	AB25	720	
3	13	–	–	–	717	
3	14	32	46	AA24	714	[1]
3	15	33	47	Y23	711	
3	16	–	–	–	708	
3	17	–	48	AC26	705	
3	18	–	–	–	702	
4	1	–	–	–	699	
4	2	2	3	E23	696	[1]
4	3	–	4	C26	693	
4	4	–	–	–	690	
4	5	3	5	E24	687	[1]
4	6	4	6	F24	684	
4	7	–	–	–	681	
4	8	5	7	E25	678	[1]
4	9	–	–	D26	675	
4	10	–	8	G24	672	
4	11	–	–	F25	669	
4	12	6	9	F26	666	[1]
4	13	–	–	–	663	
4	14	7	10	H23	660	
4	15	–	12	G26	657	
4	16	–	–	–	654	
4	17	–	14	H25	651	
4	18	–	–	–	648	

Notes: [1] Global control pin

XC95288XL I/O Pins (continued)

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
5	1	–	–	–	645	
5	2	34	49	AA23	642	
5	3	–	50	AB24	639	
5	4	–	–	–	636	
5	5	35	51	AD25	633	
5	6	–	54	AE24	630	
5	7	–	–	–	627	
5	8	38	55	AD23	624	[1]
5	9	–	–	AC22	621	
5	10	39	56	AF24	618	
5	11	–	–	AD22	615	
5	12	40	57	AE23	612	
5	13	–	–	–	609	
5	14	41	58	AE22	606	
5	15	43	60	AE21	603	
5	16	–	–	–	600	
5	17	44	61	AF21	597	
5	18	–	–	–	594	
6	1	–	–	–	591	
6	2	135	197	C19	588	
6	3	136	198	D18	585	
6	4	–	–	–	582	
6	5	137	199	A21	579	
6	6	138	200	B20	576	
6	7	–	–	–	573	
6	8	139	201	C20	570	
6	9	–	–	B21	567	
6	10	140	202	B22	564	
6	11	–	–	C21	561	
6	12	–	203	D20	558	
6	13	–	–	–	555	
6	14	142	205	B24	552	
6	15	143	206	C23	549	[1]
6	16	–	–	–	546	
6	17	–	208	D22	543	
6	18	–	–	–	540	

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
7	1	–	–	–	537	
7	2	–	62	AC19	534	
7	3	45	63	AD19	531	
7	4	–	–	–	528	
7	5	46	64	AE20	525	
7	6	–	66	AC18	522	
7	7	–	–	–	519	
7	8	–	67	AD18	516	
7	9	–	–	AE19	513	
7	10	–	69	AD17	510	
7	11	–	–	AE18	507	
7	12	48	70	AF18	504	
7	13	–	–	–	501	
7	14	–	71	AE17	498	
7	15	49	72	AE16	495	
7	16	–	–	–	492	
7	17	–	73	AF16	489	
7	18	–	–	–	486	
8	1	-	–	–	483	
8	2	130	186	A15	480	
8	3	131	187	B15	477	
8	4	–	–	–	474	
8	5	132	188	C15	471	
8	6	–	189	D15	468	
8	7	–	–	–	465	
8	8	133	191	A16	462	
8	9	–	–	B16	459	
8	10	134	192	C16	456	
8	11	–	–	B17	453	
8	12	–	193	C17	450	
8	13	–	–	–	447	
8	14	–	194	B18	444	
8	15	–	195	A20	441	
8	16	–	–	–	438	
8	17	–	196	B19	435	
8	18	–	–	–	432	

Note: [1] Global control pin

XC95288XL I/O Pins (continued)

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
9	1	–	–	–	429	
9	2	50	74	AE14	426	
9	3	51	75	AF14	423	
9	4	–	–	–	420	
9	5	52	76	AE13	417	
9	6	53	77	AC13	414	
9	7	–	–	–	411	
9	8	54	78	AD13	408	
9	9	–	–	AF12	405	
9	10	–	80	AE12	402	
9	11	56	82	AD12	399	
9	12	57	83	AC12	396	
9	13	–	–	–	393	
9	14	58	84	AF11	390	
9	15	–	85	AE11	387	
9	16	–	–	–	384	
9	17	59	86	AE9	381	
9	18	–	–	–	378	
10	1	–	–	–	375	
10	2	117	170	C10	372	
10	3	118	171	B9	369	
10	4	–	–	–	366	
10	5	119	173	A9	363	
10	6	120	174	D11	360	
10	7	–	–	–	357	
10	8	121	175	B11	354	
10	9	–	–	A11	351	
10	10	124	178	C12	348	
10	11	125	179	B12	345	
10	12	126	180	A12	342	
10	13	–	–	–	339	
10	14	128	182	A13	336	
10	15	–	183	B14	333	
10	16	–	–	–	330	
10	17	129	185	C14	327	
10	18	–	–	–	324	

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
11	1	–	–	–	321	
11	2	–	87	AD9	318	
11	3	60	88	AC10	315	
11	4	–	–	–	312	
11	5	61	89	AF7	309	
11	6	–	90	AE8	306	
11	7	–	–	–	303	
11	8	–	91	AD8	300	
11	9	–	–	AE7	297	
11	10	64	95	AD7	294	
11	11	66	97	AE5	291	
11	12	68	99	AC7	288	
11	13	–	–	–	285	
11	14	69	100	AE3	282	
11	15	–	101	AD4	279	
11	16	–	–	–	276	
11	17	70	102	AC5	273	
11	18	–	–	–	270	
12	1	–	–	–	267	
12	2	110	158	B3	264	
12	3	111	159	A3	261	
12	4	–	–	–	258	
12	5	112	160	D6	255	
12	6	–	161	C6	252	
12	7	–	–	–	249	
12	8	113	162	B5	246	
12	9	–	–	A4	243	
12	10	115	164	B6	240	
12	11	–	165	A6	237	
12	12	116	166	D8	234	
12	13	–	–	–	231	
12	14	–	167	B7	228	
12	15	–	168	A7	225	
12	16	–	–	–	222	
12	17	–	169	D9	219	
12	18	–	–	–	216	

XC95288XL I/O Pins (continued)

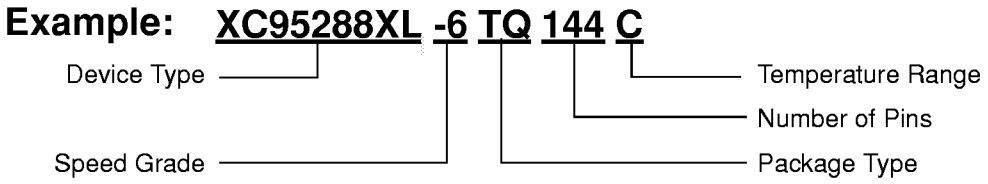
Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
13	1	–	–	–	213	
13	2	71	103	AD3	210	
13	3	–	106	AD2	207	
13	4	–	–	–	204	
13	5	–	107	AC3	201	
13	6	–	109	AD1	198	
13	7	–	–	–	195	
13	8	74	110	AA4	192	
13	9	–	–	AA3	189	
13	10	–	111	AB2	186	
13	11	75	112	AC1	183	
13	12	–	113	AA2	180	
13	13	–	–	–	177	
13	14	76	114	AA1	174	
13	15	77	115	Y1	171	
13	16	–	–	–	168	
13	17	78	116	V4	165	
13	18	–	–	–	162	
14	1	–	–	–	159	
14	2	–	144	K3	156	
14	3	100	145	G1	153	
14	4	–	–	–	150	
14	5	101	146	H2	147	
14	6	102	147	H3	144	
14	7	–	–	–	141	
14	8	103	148	J4	138	
14	9	–	–	F1	135	
14	10	104	149	G2	132	
14	11	105	150	G3	129	
14	12	–	151	F2	126	
14	13	–	–	–	123	
14	14	106	152	E2	120	
14	15	107	154	D2	117	
14	16	–	–	–	114	
14	17	–	155	F4	111	
14	18	–	–	–	108	

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
15	1	–	–	–	105	
15	2	79	117	V3	102	
15	3	80	118	W2	99	
15	4	–	–	–	96	
15	5	–	119	U4	93	
15	6	–	120	U3	90	
15	7	–	–	–	87	
15	8	81	121	V2	84	
15	9	–	–	V1	81	
15	10	82	122	U2	78	
15	11	83	123	T2	75	
15	12	85	125	R4	72	
15	13	–	–	–	69	
15	14	86	126	R3	66	
15	15	87	127	R2	63	
15	16	–	–	–	60	
15	17	88	128	R1	57	
15	18	–	–	–	54	
16	1	–	–	–	51	
16	2	91	131	P1	48	
16	3	92	133	N2	45	
16	4	–	–	–	42	
16	5	93	134	N4	39	
16	6	94	135	N3	36	
16	7	–	–	–	33	
16	8	95	136	M1	30	
16	9	–	–	M2	27	
16	10	96	137	M3	24	
16	11	97	138	M4	21	
16	12	98	139	L1	18	
16	13	–	–	–	15	
16	14	–	140	L2	12	
16	15	–	142	L3	9	
16	16	–	–	–	6	
16	17	–	143	J1	3	
16	18	–	–	–	0	

XC95288XL Global, JTAG and Power Pins

Pin Type	TQ144	PQ208	BG352
I/O/GCK1	30	44	Y24
I/O/GCK2	32	46	AA24
I/O/GCK3	38	55	AD23
I/O/GTS1	5	7	E25
I/O/GTS2	6	9	F26
I/O/GTS3	2	3	E23
I/O/GTS4	3	5	E24
I/O/GSR	143	206	C23
TCK	67	98	AD6
TDI	63	94	AF6
TDO	122	176	D12
TMS	65	96	AE6
V_{CCINT} 3.3V	8, 42, 84, 141	11, 59, 124, 153, 204	J23, V24, AF23, AC15, AF15, AD11, AD5, Y3, T1, J3, G4, D5, D10, B13, D17, C22, H24
V_{CCIO} 2.5V/3.3 V	1, 37, 55, 73, 109, 127	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184	A10, A17, B2, B25, D7, D13, D19, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC8, AC14, AC20, AE25, AF10, AF17
GND	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	2, 13, 24, 27, 42, 52, 68, 81, 93, 104,1 08, 129, 130, 141, 156, 163, 177, 190, 207	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, C7, C9, C13, C18, D24, E1, E26, H1, H26, K4, N1, N24, P3, P26, V23, W1, W4, W26, AB1, AB4, AB26, AC9, AD10, AD14, AD15, AD20, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26
No Connects	–	–	A18, A23, A24, B4, B8, B10, B23, C1, C2, C3, C4, C5, C8, C11, C24, C25, D1, D3, D4, D14, D16, D21, D23, D25, E3, E4, F3, F23, G25, J2, J24, J26, K2, L4, L23, P2, T3, T4, T24, U25, V25, W3, W24, Y2, AB3, AB23, AC2, AC4, AC6, AC11, AC16, AC17, AC21, AC23, AC24, AC25, AD16, AD21, AD24, AD26, AE2, AE4, AE10, AE15, AF3, AF4, AF9, AF20

Ordering Information



Speed Options

-10 10 ns pin-to-pin delay
-6 6 ns pin-to-pin delay

Packaging Options

TQ144 144-Pin Thin Quad Flat Pack (TQFP)
PQ208 208-Pin Plastic Quad Flat Pack (PQFP)
BG352 352-Pin Plastic Ball Grid Array (BGA)

Temperature Options

C= Commercial T_A = 0°C to +70°C
I = Industrial T_A = -40°C to +85°C

Component Availability

Pins		144	208	352
Type		**Plastic TQFP**	**Plastic PQFP**	**Plastic BGA**
Code		**TQ144**	**PQ208**	**BG352**
XC95288XL	-10	C, I	C, I	(C)
	-6	(C)	(C)	(C)

C = Commercial (T_A = 0°C to +70°C) I = Industrial (T_A = -40°C to +85°C)
( ) Parenthesis indicate future product plans. Please contact Xilinx for up-to-date availability information.